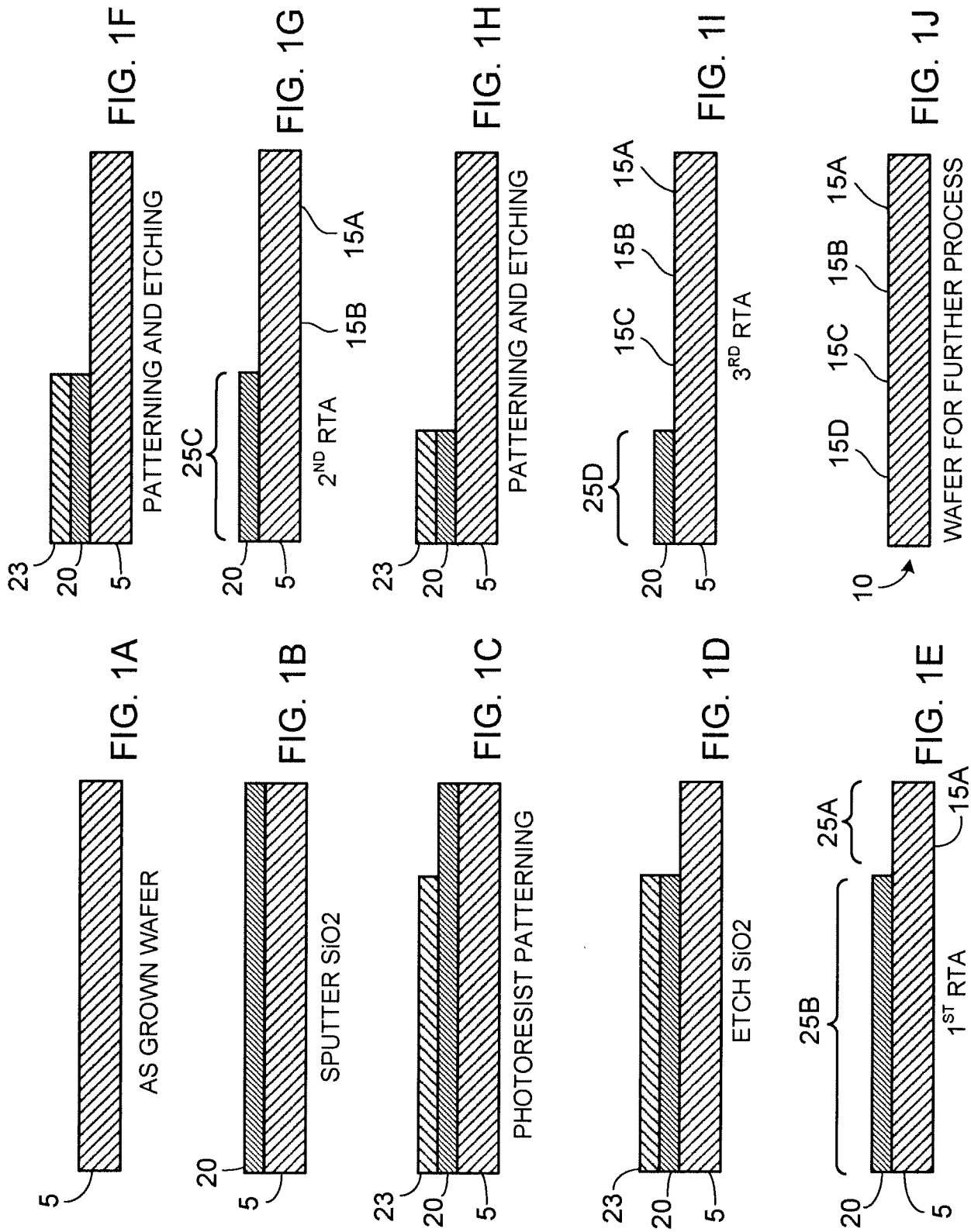


FIG. 1A
AS GROWN WAFER
5
FIG. 1B
SPUTTER SiO2
20
5
FIG. 1C
PHOTORESIST PATTERNING
23
20
5
FIG. 1D
ETCH SiO2
23
20
5
FIG. 1E
1ST RTA
25B
25A
15A
20
5
FIG. 1F
PATTERNING AND ETCHING
23
20
5
FIG. 1G
2ND RTA
25C
15B
15A
20
5
FIG. 1H
PATTERNING AND ETCHING
23
20
5
FIG. 1I
3RD RTA
25D
15C
15B
15A
20
5
FIG. 1J
WAFER FOR FURTHER PROCESS
15D
15C
15B
15A
10

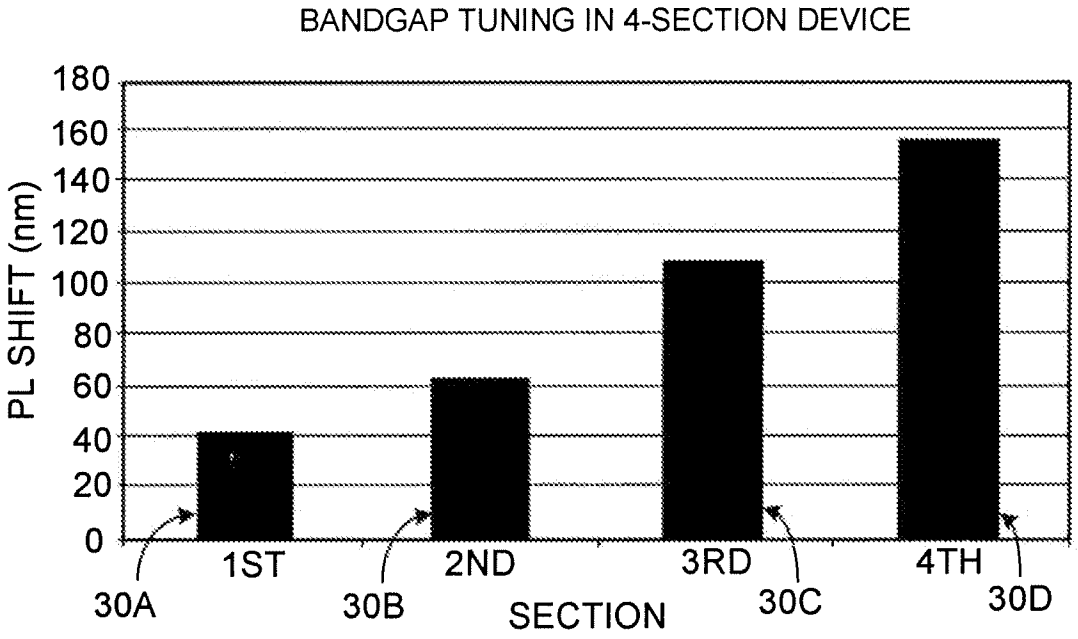
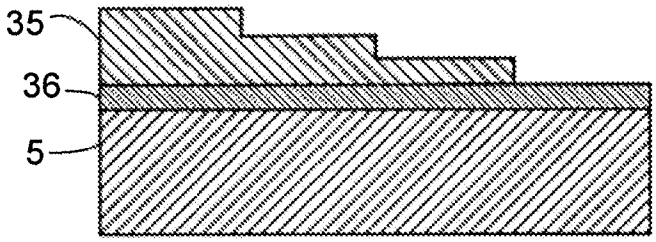
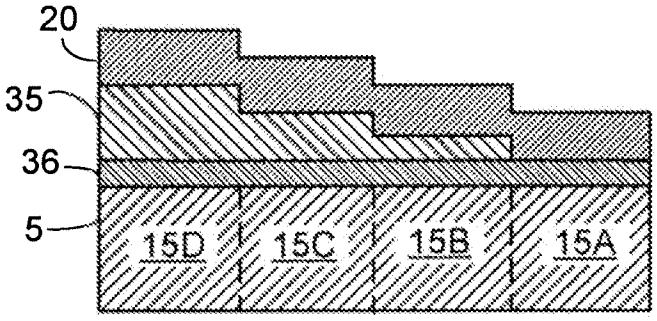

BANDGAP TUNING IN 4-SECTION DEVICE
PL SHIFT (nm)
180
160
140
120
100
80
60
40
20
0
1ST
2ND
3RD
4TH
30A
30B
SECTION
30C
30D

FIG. 2



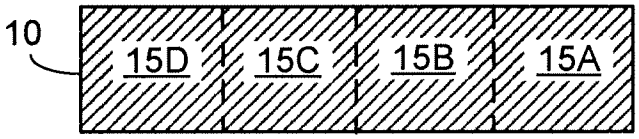
A) PATTERNING OF THE AS-GROWN WAFER

FIG. 3A



B) PATTERNING OF THE AS-GROWN WAFER, DIELECTRIC CAP DEPOSITION AND RTA

FIG. 3B



C) REMOVE ALL SACRIFICIAL LAYERS FOR FURTHER PROCESSING OF THE DEVICE WAFER

FIG. 3C

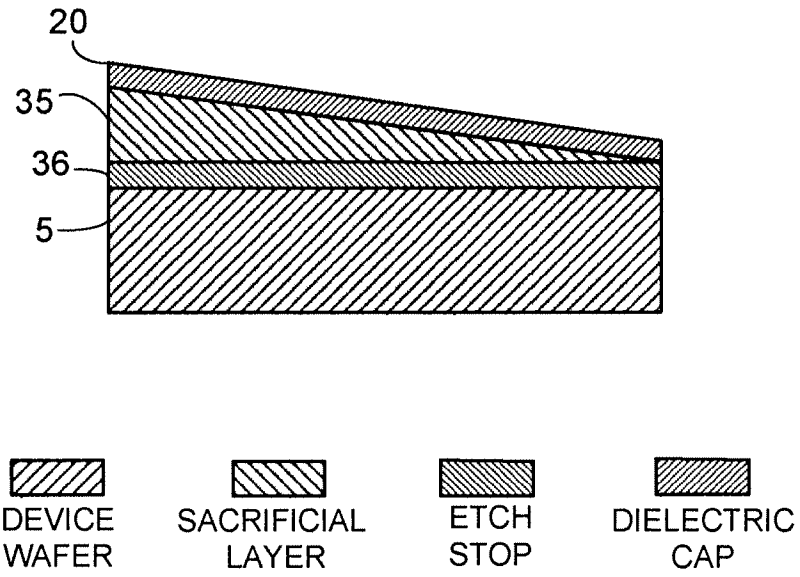

20
35
36
5
DEVICE WAFER
SACRIFICIAL LAYER
ETCH STOP
DIELECTRIC CAP

FIG. 4

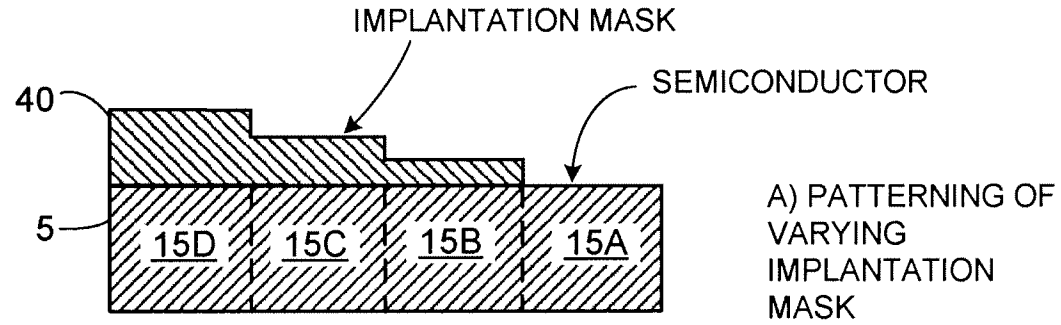


FIG. 5A

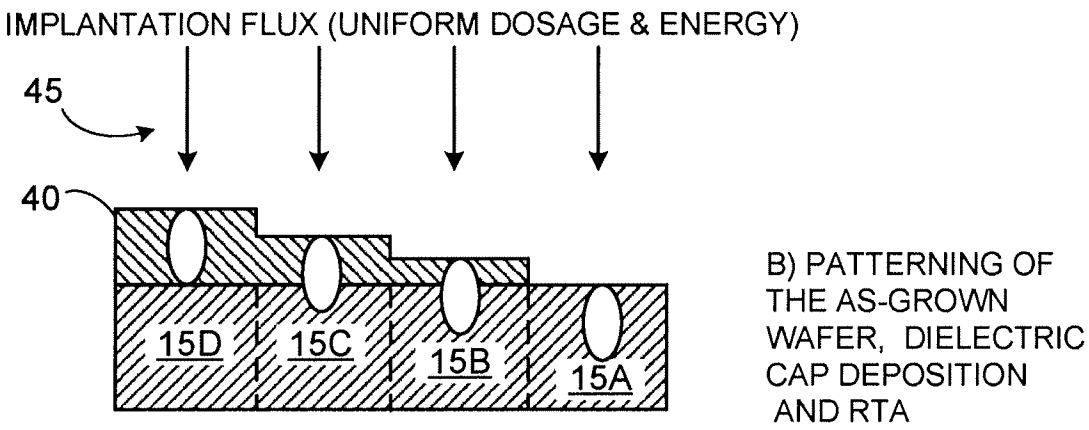


FIG. 5B

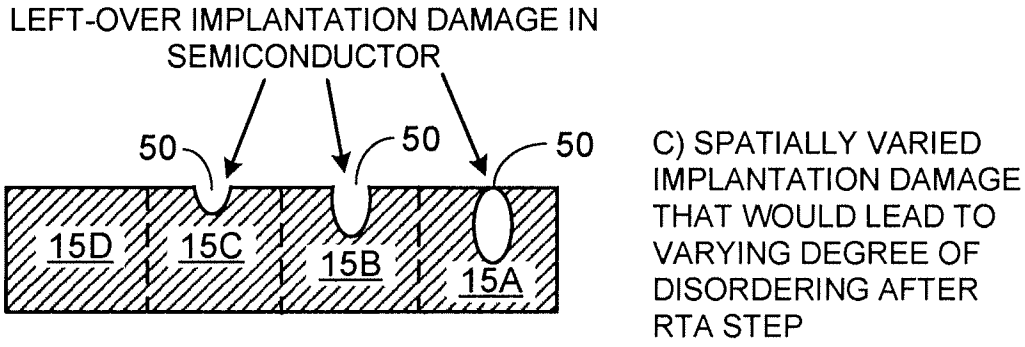


FIG. 5C

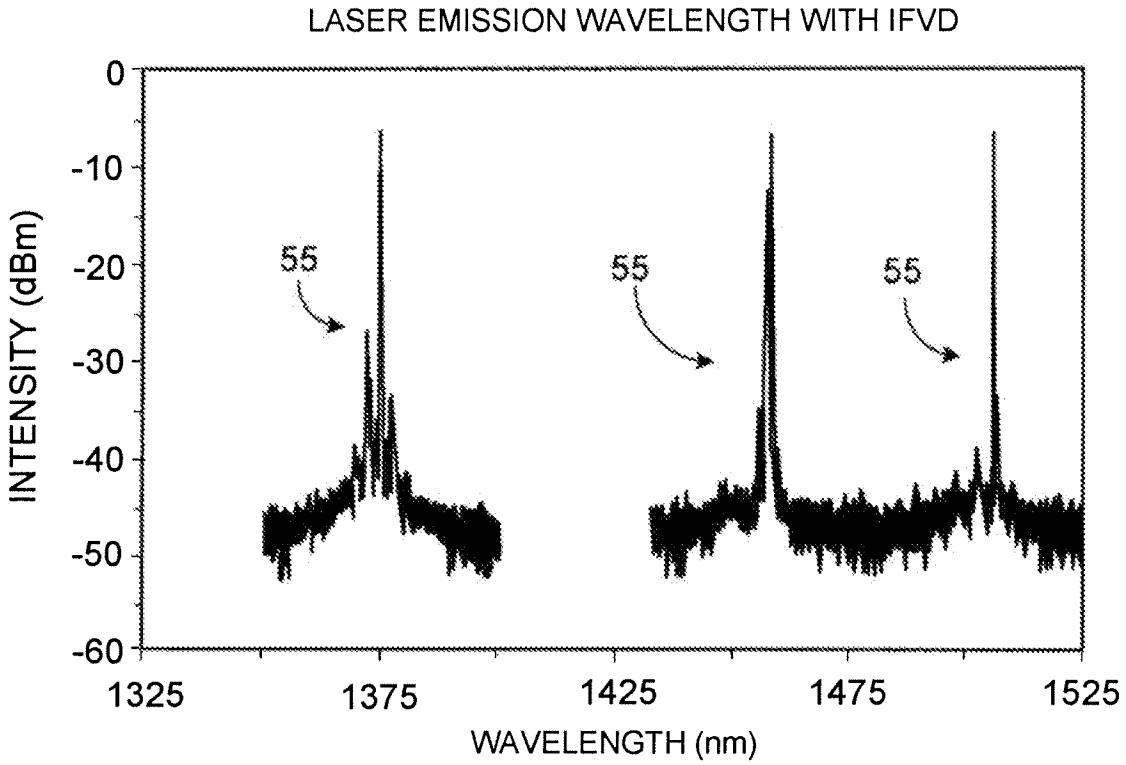

LASER EMISSION WAVELENGTH WITH IFVD
INTENSITY (dBm)
0
-10
-20
-30
-40
-50
-60
55
55
55
1325
1375
1425
1475
1525
WAVELENGTH (nm)

FIG. 6

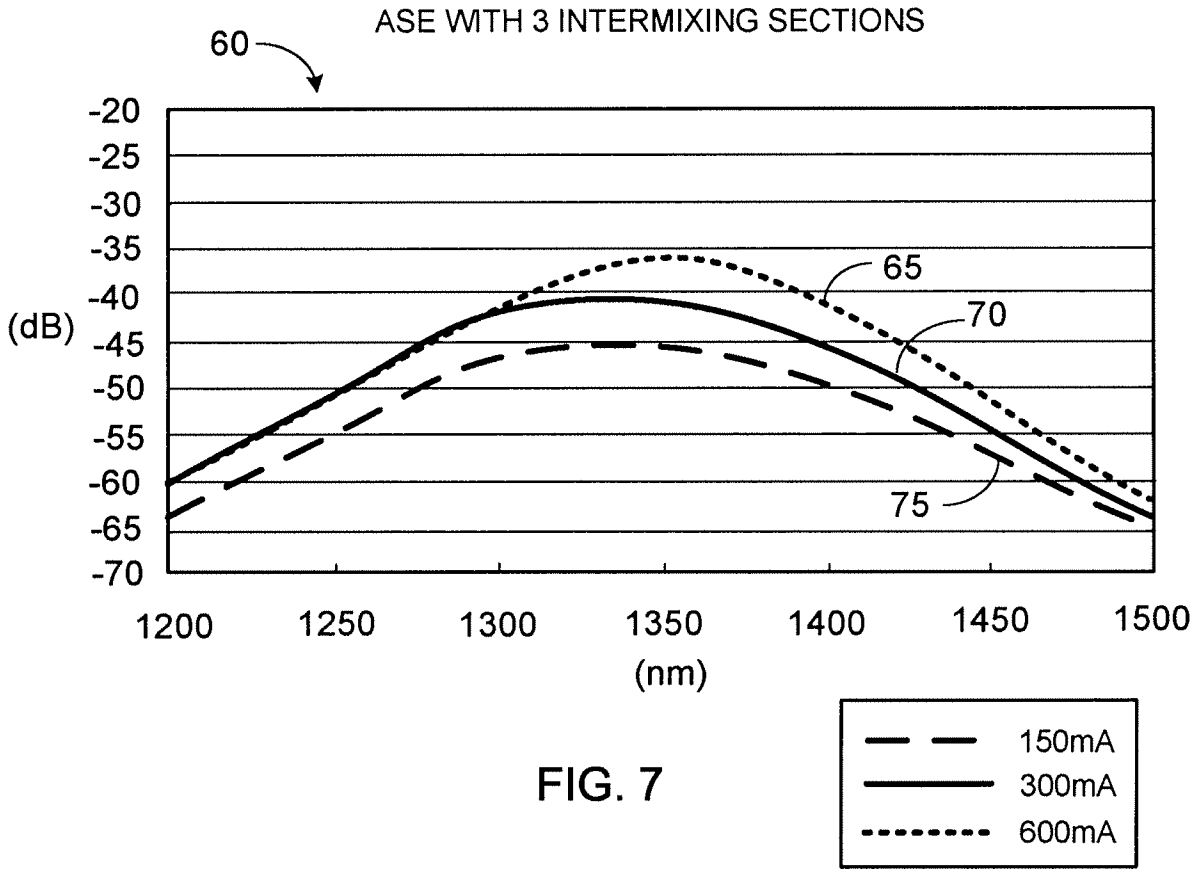

ASE WITH 3 INTERMIXING SECTIONS
60
-20
-25
-30
-35
-40
-45
-50
-55
-60
-65
-70
(dB)
65
70
75
1200
1250
1300
1350
1400
1450
1500
(nm)
150mA
300mA
600mA

FIG. 7

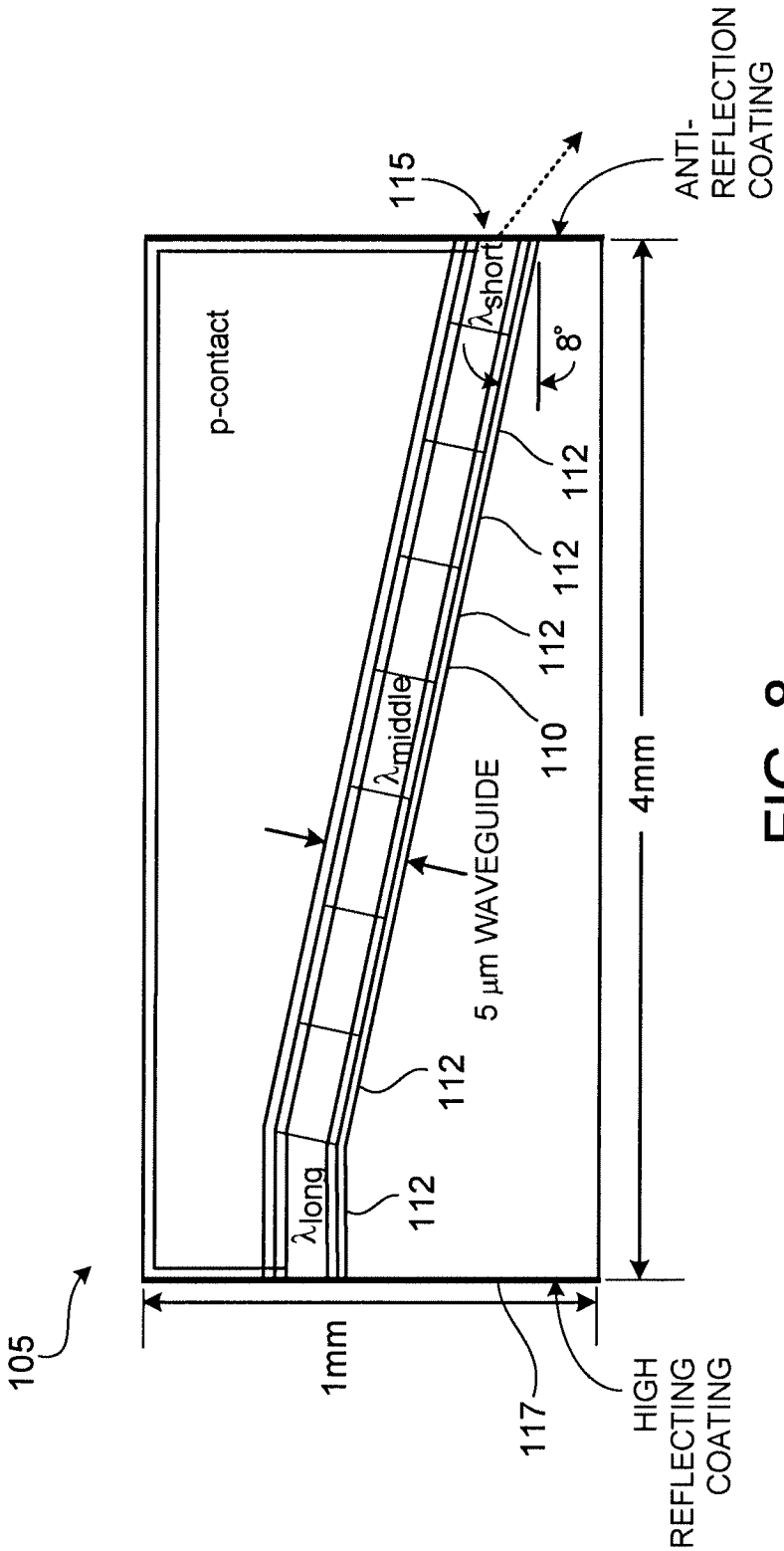

ANTI-
REFLECTION
COATING
115
p-contact
λ_{short}
8°
112
112
112
λ_{middle}
110
5 μm WAVEGUIDE
4mm
112
112
λ_{long}
105
1mm
117
HIGH
REFLECTING
COATING

FIG. 8